AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method in a computer system having a global descriptor table register for executing code during a system management mode interrupt (SMI), the method comprising:

upon occurrence of the SMI,

saving state of the computer system;

switching the computer system to protected mode;

replacing first contents of the global descriptor table register that point to a first global descriptor table in use when the system management mode interrupt occurred with second contents that point to a second global descriptor table that is distinct from the first global descriptor table;

executing 32-bit code using the second global descriptor table; and

upon completion of the execution of the 32-bit code,

restoring the saved state of the computer system; and

returning from the occurrence of the SMI.

2. (Previously Presented) The method of claim 1 wherein the 32-bit code is an operating system kernel for loading and running programs during the occurrence of the system management mode interrupt.

3. (Previously Presented) The method of claim 2 wherein the programs are Windows Portable Executable programs.

4. (Previously Presented) The method of claim 1 wherein the computer system is based on an Intel Pentium processor.

5-11 (Canceled).

12. (Currently Amended) The method of ~~claim 5~~claim 1 wherein the computer system is based on an Intel-compatible processor.

13. (Currently Amended) The method of ~~claim 5~~claim 1 wherein the ~~executed~~ 32-bit code is selected from the group consisting of a remote console program, a remote boot program, a remote diagnostics program, a remote restart program, and a debugging program.

14. (Canceled).

15. (Currently Amended) The method of ~~claim 5~~claim 1 wherein the computer system has a foreground operating system, and wherein the 32-bit code executes transparently to the foreground operating system.

16. (Currently Amended) The method of ~~claim 5~~claim 1 wherein the computer system has a foreground operating system, and wherein the 32-bit code executes even if the foreground operating system has crashed or stopped.

17. (Currently Amended) The method of ~~claim 5~~claim 1 wherein the computer system has a foreground operating system, and wherein the 32-bit code executes when the foreground operating system crashes or stops.

18-23 (Canceled).

24. (Currently Amended) The ~~computer-readable medium of claim 18~~method of claim 1 wherein the ~~Portable Executable program~~32-bit code is loaded into memory from a ROM.

25. (Currently Amended) The ~~computer-readable medium of claim 18~~method of claim 1 wherein the ~~Portable Executable program~~32-bit code is loaded into memory from a Flash ROM.

26. (Previously Presented) The method of claim 1 wherein a processor switches to system management mode and executes the SMI in response to a signal received on an input line of the processor.

27. (Previously Presented) The method of claim 26 wherein the input line is an SMI input line.

28. (Canceled)

29. (Previously Presented) The method for claim 1 wherein a processor switches to system management mode and executes the SMI in response to a message received via a front side bus of the processor.

30. (Previously Presented) The method of claim 1 wherein a processor chip set is the source of the SMI.

31. (Previously Presented) The method of claim 1 wherein a Northbridge controller is the source of the SMI.

32. (Previously Presented) The method of claim 1 wherein a Southbridge controller is the source of the SMI.

33. (Previously Presented) The method of claim 1 wherein an electronic circuit is the source of the SMI.

34. (Previously Presented) The method of claim 1 wherein returning from the occurrence of the interrupt is accomplished by executing an RSM instruction.

35-56 (Canceled).

57. (New) A computer system comprising:

a global descriptor table register for executing code during a system management mode interrupt (SMI); and

a component to receive the SMI and, upon receiving the SMI, cause the computer system to perform the steps of:

saving state of the computer system;

switching the computer system to protected mode;

replacing first contents of the global descriptor table register that point to a first global descriptor table in use when the system management mode interrupt occurred with second contents that point to a second global descriptor table that is distinct from the first global descriptor table;

executing 32-bit code using the second global descriptor table; and

upon completion of the execution of the 32-bit code,

restoring the saved state of the computer system; and

returning from the occurrence of the SMI.

58. (New) The computer system of claim 57 further comprising an operating system kernel for loading and running programs during the occurrence of the SMI.

59. (New) The computer system of claim 58 wherein the programs are portable executables.

60. (New) The computer system of claim 57 wherein the computer system is based on an Intel processor.

61. (New) The computer system of claim 57 wherein the computer system is based on an Intel-compatible processor.

62. (New) The computer system of claim 57 wherein the 32-bit executed code is selected from the group consisting of a remote console program, a remote boot program, a remote diagnostics program, a remote restart program, and a debugging program.

63. (New) The computer system of claim 57 wherein the computer system has a foreground operating system, and wherein the 32-bit code executes transparently to the foreground operating system.

64. (New) The computer system of claim 57 wherein the computer system has a foreground operating system, and wherein the 32-bit code executes even if the foreground operating system has crashed or stopped.

65. (New) The computer system of claim 57 wherein the computer system has a foreground operating system, and wherein the 32-bit code executes when the foreground operating system crashes or stops.

67. (New) The computer system of claim 57 wherein the SMI is received in response to a signal received on an input line of the computer system.

68. (New) The computer system of claim 67 wherein the input line is an SMI input line.

69. (New) The computer system of claim 57 wherein the SMI is received in response to a message received via a front side bus of the computer system.

70. (New) The computer system of claim 57 wherein a processor chip set is the source of the SMI.

71. (New) The computer system of claim 57 wherein a Northbridge controller is the source of the SMI.

72. (New) The computer system of claim 57 wherein a Southbridge controller is the source of the SMI.

73. (New) The computer system of claim 57 wherein an electronic circuit is the source of the SMI.

74. (New) The computer system of claim 57 wherein the computer system returns from the occurrence of the SMI by executing an RSM instruction.

75. (New) A computer-readable storage medium encoded with a global descriptor table register for executing code during a system management mode interrupt (SMI) and instructions that, when executed by a computer upon occurrence of the SMI, cause the computer to:

save a state of the computer;

switch the computer to protected mode;

replace first contents of the global descriptor table register that point to a first global descriptor table in use when the SMI occurred with second contents that point to a second global descriptor table that is distinct from the first global descriptor table;

execute 32-bit code using the second global descriptor table; and

upon completion of the execution of the 32-bit code,

restore the saved state of the computer; and

return from the occurrence of the SMI.

76. (New) The computer-readable storage medium of claim 75 wherein the computer includes a Pentium-based processor.

77. (New) The computer-readable storage medium of claim 75 wherein the instructions are loaded into system management memory by a BIOS.

78. (New) The computer-readable storage medium of claim 75 wherein the 32-bit code is loaded into memory from a ROM.

79. (New) The computer-readable storage medium of claim 75 wherein the 32-bit code is loaded into memory from a Flash ROM.

80. (New) The computer-readable storage medium of claim 75 wherein a processor switches to system management mode and executes the SMI in response to a signal received on an input line of the processor.

81. (New) The computer-readable storage medium of claim 80 wherein the input line is an SMI input line.

82. (New) The computer-readable storage medium of claim 75 wherein a processor switches to system management mode and executes the SMI in response to a message received via a front side bus of the processor.

83. (New) The computer-readable storage medium of claim 75 wherein a processor chip set is the source of the SMI.

84. (New) The computer-readable storage medium of claim 75 wherein a Northbridge controller is the source of the SMI.

85. (New) The computer-readable storage medium of claim 75 wherein a Southbridge controller is the source of the SMI.

86. (New) The computer-readable storage medium of claim 75 wherein an electronic circuit is the source of the SMI.

87. (New) The computer-readable storage medium of claim 75 further comprising instructions that cause the computer to return from the SMI by executing an RSM instruction.